

Serial No. 10/612,333  
Docket: MIO 0022 V2/ 40509.257

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AMENDMENT TO THE CLAIMS

1. (Original) A method of manufacturing a memory cell comprising an electrically conductive word line, an electrically conductive bit line, an electrical charge storage structure, a transistor structure, and a bit line contact, said method comprising the steps of:

forming said charge storage structure so as to be conductively coupled to said bit line via said transistor structure and said bit line contact;

forming said transistor structure so as to be conductively coupled to said word line;

forming said bit line contact by forming a conductively doped polysilicon plug within a contact hole bounded by insulating side walls; and

forming said doped polysilicon plug so as to define a substantially convex upper plug surface profile in contact with said bit line.

2. (Currently Amended) A method of manufacturing a memory cell as claimed in claim 1 wherein said insulating side walls are formed so as to comprise a first pair of opposing insulating side walls along said-a first dimension and a second pair of opposing insulating side walls along said-a second dimension.

3. (Original) A method of manufacturing a memory cell as claimed in claim 2 wherein said first pair of opposing insulating side walls are formed so as to comprise respective layers of insulating spacer material formed over a conductive line.

4. (Original) A method of manufacturing a memory cell as claimed in claim 2 wherein said second pair of opposing insulating side walls are formed so as to comprise respective layers of insulating material formed between respective contact holes.

5. (Original) A method of manufacturing a memory cell as claimed in claim 1 wherein said contact hole is filled with said polysilicon plug to an uppermost extent of said insulating side walls.

6-18. (Canceled)